REMARKS

This paper is being provided in response to the Office Action dated January 28, 2008, received for the above-referenced application. In this response, Applicants have amended claims 1, 5, 10, 13, 15 and 19 to clarify that which Applicants consider to be the presently-claimed invention. Applicants respectfully submit that the amendments to the claims are fully supported by the originally-filed specification.

The rejection of claims 5, 13 and 19 under 35 U.S.C. 112, second paragraph, as being indefinite has been addressed by amendments contained herein in accordance with the guidelines set forth in the Office Action. Accordingly, Applicants respectfully request that the rejection be reconsidered and withdrawn.

The rejection of claims 1, 2, 7-11, 13, 15, 16 and 18 under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 7,043,623 by Chen, et al. (hereinafter "Chen") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein. Applicants believe that this rejection is actually being asserted under 35 U.S.C 102(e), instead of the identified 102(a).

Independent claim 1, as amended herein, recites a method of accessing data memory including writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored. In response to a request to read data from the memory address, data is read from the first memory location or the second memory location

based on load balancing. Tests are run to determine if one of the first memory location and the second memory location has failed. In response to failure of one of the first and second memory locations, the method provides for transitioning into a failover state and causing a non-failed one of the first memory location and the second memory location to be a primary memory location. Date is accessed from the primary memory location in response to a request while in the failover state to access data at the memory address. Claims 2-9 depend directly or indirectly from independent claim 1.

Independent claim 10, as amended herein, recites computer software, stored in a computer-readable medium, that accesses data memory including machine executable code that writes data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored. Machine executable code reads data from the first memory location or the second memory location based on load balancing in response to a request to read data from the memory address. Machine executable code runs tests to determine if one of the first memory location and the second memory location has failed. Machine executable code transitions into a failover state and causes a non-failed one of the first memory location and the second memory location to be a primary memory location in response to failure of one of the first and second memory locations. Machine executable code that accesses data from the primary memory location in response to a request while in the failover state to access data at the memory address. Claims 11-14 depend directly or indirectly from independent claim 10.

Independent claim 15, as amended herein, recites a data storage device including a plurality of disk drives, an internal volatile memory, and a plurality of directors coupled to the memory. Some of the directors are coupled to the disk drives and some of the directors allow external access to the data storage device and wherein each of the directors access the memory by writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored. In response to a request to read data from the memory address, the directors read data from the first memory location or the second memory location based on load balancing. The directors run tests to determine if one of the first memory location and the second memory location has failed, the directors transition into a failover state and cause a non-failed one of the first memory location and the second memory location to be a primary memory location in response to failure of one of the first and second memory locations. The directors access data from the primary memory location in response to a request while in the failover state to access data at the memory address. Claims 16-20 depend directly or indirectly from independent claim 15.

The Chen reference discloses a distributed memory computing environment and implementation. The Office Action cites principally to col. 8, lines 25-65 of Chen, and Figures 4 and 19, as disclosing mirroring of memory and including use of a load balancing algorithm to redirect memory access requests ("malloc", "read", "write", "delete") to another server.

Applicants' independent claims, as amended herein, recite method and systems for accessing data memory that include at least the features of running tests to determine if one of

the first memory location and the second memory location has failed, in response to failure of one of the first and second memory locations, transitioning into a failover state and causing a non-failed one of the first memory location and the second memory location to be a primary memory location, and accessing data from the primary memory location in response to a request while in the failover state to access data at the memory address. (See, for example, page 30, line 6 to page 31, line 3 of the originally-filed specification). Applicants respectfully submit that at least the above-noted features are not taught nor fairly suggested by Chen.

Specifically, at col. 8, lines 43-52 and Fig. 4 and also the discussion in connection with Fig. 19 at col. 14, lines 28-47, Chen discloses a backup and recovery scheme involving the replacement of a failed Network Attached Memory (NAM) with a new NAM and including the designation of one NAM as a NAM Dispatcher to examine all memory requests and provide for automatic fault tolerance and scalability. However, Applicants respectfully submit that Chen does not disclose that in response to failure determined from the running of tests to determined failure, transitioning into a failover state and then designating one of the memory locations as a primary memory location to which access is allowed in response to a request to access data while in the failover state. Instead, Chen discloses that one NAM, already designated, examines all memory requests, and does not disclose a response to a failure by transitioning to a failover state, designating, in response the failure, of one of the memory locations as a primary memory location and allowing access to the primary memory location in response to requests to access data while in the failover state, as claimed by Applicants. Accordingly, in view of the above, Applicants respectfully request that the rejection be reconsidered and withdrawn.

The rejection of claims 3, 12 and 17 under 35 U.S.C. 103(a) as being unpatentable over Chen is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

The features of independent claims 1, 10 and 15 are discussed above. Claims 3, 12 and 17 depend therefrom. Applicants refer to the discussion above concerning Chen with respect to Applicants' independent claims, as amended herein, and submit that Chen does not teach or fairly suggest at least the above-noted features as claimed by Applicants. In view of the above, Applicants respectfully request that the rejection be reconsidered and withdrawn.

The rejection of claims 6, 14 and 20 under 35 U.S.C. 103(a) as being unpatentable over Chen in view of U.S. Patent No. 6,052,308 to Pitts (hereinafter "Pitts") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein. Applicants note that the bottom of page 5 of the Office Action indicates at one location that "Claims 4, 14 and 120" are being rejected; however, the paragraph thereafter clarifies that the rejection stated therein is being applied with respect to claims 6, 14 and 20.

Independent claims 1, 10 and 15 are discussed above in connection with Chen. Claims 6, 14 and 20 depend therefrom.

The Pitts reference discloses a balanced sensing arrangement for flash EEPROM. The Office Action cites to Pitts as disclosing toggling in a multiplexer between two different states so

that data accessing is balanced between an upper memory cell and a low memory cell of a read only memory.

Applicants respectfully submit that Pitts does not overcome the above-noted deficiencies of Chen with respect to Applicant's presently-claimed invention. Specifically, Applicants respectfully submit that neither Chen nor Pitts, taken alone or in combination, teach or fairly suggest a method and systems for accessing data memory that include at least the features of for a mirrored first memory location and second memory location, running tests to determine if one of a first memory location and a second memory location has failed, in response to failure of one of the first and second memory locations, transitioning into a failover state and causing a non-failed one of the first memory location and the second memory location to be a primary memory location, and accessing data from the primary memory location in response to a request while in the failover state to access data at the memory address, as claimed by Applicants. In view of the above, Applicants respectfully request that the rejection be reconsidered and withdrawn.

With respect to the rejections using U.S. Patent App. Pub. No. 2004/0205384 to Lai et al. (hereinafter "Lai"), as set forth below, Applicants reiterate arguments concerning removal of the Lai reference as invalidly applied to reject the presently-claimed invention. Applicants note, in particular, the additional discussion of the Exhibit A that has been incorporated hereinbelow along with additional comments concerning the 131 Declaration and Exhibit A in view of amendments to the claims contained herein.

The rejection of claims 1-6 and 10-14 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent App. Pub. No. 2004/0205384 to Lai et al. (hereinafter "Lai") in view of Pitts, the rejection of claims 7-9 under 35 U.S.C. as being unpatentable over Lai in view of Pitts and further in view of U.S. Patent App. Pub. No. 2005/0160311 to Hartwell, et al. (hereinafter "Hartwell"), and the rejection of claims 15-20 under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Hartwell and further in view of Pitts, are all hereby traversed in view of the previously-submitted Declaration under 37 C.F.R. 1.131, as further detailed below.

The Lai reference is a published U.S. patent application that was filed in the United States on February 18, 2004, and published on October 14, 2004. The present above-captioned patent application to Cartmell, et al. (hereinafter "the present patent application") was filed in the United States on March 29, 2004. Accordingly, the Lai reference is prior art under 35 U.S.C. 102(e).

Applicants has previously submitted a Declaration under 37 C.F.R. 1.131 that has been executed by all the inventors (hereinafter "the 131 Declaration") to swear-behind, and thereby remove, the Lai reference as applied against the presently-claimed invention. The Office Action (bottom of page 14, top of page 15) indicates Applicants, in the response dated October 16, 2007, merely repeat same arguments concerning the 131 Declaration and refers to the Office Action dated July 16, 2007. However, Applicants responded in the response filed October 16, 2007 to the statement that Applicant should provide a clear explanation of the exhibits pointing out what facts are established and relied on by applicant and point out that the last response was not mere repetition (see, in particular, pages 12-13 of Applicants' October 16, 2007 response). This has

been done even though, as has been pointed out by Applicants, tracking of the claim language against an exhibit is not required under MPEP 715.07(I), and instead all of the evidence must be considered in its entirety, including the Rule 131 declaration itself, accompanying exhibits, and other written record in establishing conception. Notwithstanding the above-noted portion of the MPEP, Applicants have provided additional remarks herein concerning the Exhibit A, specifically tracking features in the claims as amended. For the convenience of the Examiner, Applicants have incorporated hereinbelow portions of the additional remarks submitted in the October 16, 2007 response which included further explanatory comments concerning the 131 Declaration and supporting Exhibit A addressing conception of the presently-claimed invention, along with additional remarks concerning the Exhibit A with respect to the present claims as amended herein.

Exhibit A is a copy of a thirty-one page powerpoint-style presentation made by the inventors of the present application at an EMC internal meeting before February 18, 2004. The presentation is entitled "Symm7 Mirrored Memory Conceptual Review." Applicants submit that statements in the declaration itself and Exhibit A support a method and computer software stored in a computer-readable medium of accessing data memory, including writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored. (See, for example, the schematic on page 4 of the Exhibit A, showing an implementation of mirrored memory, flow charts on page 11 and 12 addressing 6 different mirrored memory system states, the discussion of the failed memory detection on page 20 including discussion of the functioning of the Global Memory Access (GMA) layer, and page 16

describing in more detail the GMA layer which is "responsible for maintaining the mirrored memory states" and which tells "the driver to write the data to both location"). In response to a request to read data from the memory address, data is read from the first memory location or the second memory location based on load balancing. (See, for example, the flow diagram on page 14 discussing memory access functional layering and functioning of the GMA layer application programming interface (API), and page 16 that specifies that "The GMA layer is where the read load balancing algorithm lives"). Tests are run to determine if one of the first memory location and the second memory location has failed (See, for example, in Exhibit A, the flow diagram for failed memory detection on page 20, including the running of tests on the memory). In response to failure of one of the first and second memory locations, the method includes transitioning into a failover state and causing a non-failed one of the first memory location and the second memory location to be a primary memory location. (See, for example, the flow diagrams on pages 26 and 29 concerning operations of the six different mirrored memory system states; page 19 addressing a failed memory detection state including a discussion of memory failure detection and diagnosis, and page 16 concerning operation of the GMA layer in normal and degraded mode involving a single memory location). Data is accessed from the primary memory location in response to a request while in the failover state to access data at the memory address. (See, for example, the flow diagram on page 20 showing the functioning of the GMA layer in response to a failed memory detection, and page 19 that specifies "The memory failure detection is encapsulated in the GMA layer"). Applicants also note the disclosure in the Exhibit A of a data storage device including disk drives, an internal volatile memory; and directors coupled to the memory, in relation to the above-noted functionalities (see, for example, the discussion of mirrored memory hardware implementation on page 4).

The Office Action has rejected Applicants' claims using a reference that Applicants are entitled to have removed under 37 C.F.R. 1.131. Applicants have provided extensive evidence, facts and supporting exhibits that all indicate Applicants conceived of the presently-claimed invention before the effective prior art date of the Lai reference (February 18, 2004) and were diligent until the constructive reduction to practice of the invention by the filing of the present patent application on March 29, 2004. In accordance with MPEP 715.07(I) and the case law cited therein, Applicants have adequately demonstrated conception of the claimed invention through the specific factual statements in the 131 Declaration signed by all of the inventors, including facts concerning and relating to the conception and development of the claimed invention by the inventors, the submitted 31-page Exhibit A of a presentation on Symm7 Mirrored Memory that supports the factual statements of the inventors, and the specific explanatory statements concerning the Exhibit A with respect to the presently-claimed invention that are included in the 131 Declaration itself and in the Responses to Office Actions filed by Applicants on June 22, 2006; December 14, 2006; and October 16, 2007, along with the comments now included in the present response.

Accordingly, Applicants submit that the 131 Declaration, including supporting exhibits, provides facts clearly sufficient to establish conception of the presently-claimed invention prior to the February 18, 2004, effective date of the Lai reference and establish due diligence by the inventors from a time prior to February 18, 2004, until the invention was constructively reduced to practice by the filing of the present patent application on March 29, 2004. Applicants submit that the written record is extensive on this issue in view of all of the above-noted documents and

remarks that have been submitted in this application with respect to the 131 Declaration. The result of this extensive written record is that Applicants are entitled to swear-behind the approximate month and a half that is need to the remove the rejections that use the Lai reference as prior art against the presently-claimed invention.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 508-898-8603.

Respectfully submitted,
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